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TMS320C6000 DSP Peripherals Overview

This document provides an overview and briefly describes the peripherals available on the TMS320C6000™ family of digital signal processors (DSPs).

1 Overview

The C6000™ platform of devices consists of the first off-the-shelf DSPs that use advanced very long instruction word (VLIW) to achieve high performance through increased instruction-level parallelism. The VelociTI™ VLIW architecture uses multiple execution units operating in parallel to execute multiple instructions during a single clock cycle. Parallelism is the key to extremely high performance, taking these DSPs well beyond the performance capabilities of traditional designs.

The user-accessible peripherals available on the C6000 devices are configured using a set of memory-mapped control registers. The peripheral bus controller performs the arbitration for accesses of on-chip peripherals.

Peripherals available on the TMS320C62x™ devices and their associated literature number are listed in Table 1.

Peripherals available on the TMS320C64x™ devices and their associated literature number are listed in Table 2 (page 7).

Peripherals available on the TMS320C67x™ devices and their associated literature number are listed in Table 3 (page 3).
### Table 1. TMS320C62x DSP Peripherals Documentation

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Acronym</th>
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Table 2.  TMS320C64x DSP Peripherals Documentation

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### Table 3. TMS320C67x DSP Peripherals Documentation

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<tr>
<td>Enhanced Direct Memory Access Controller</td>
<td>EDMA</td>
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<tr>
<td>External Memory Interface</td>
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<td>General-Purpose Input/Output</td>
<td>GPIO</td>
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<td>Host Port Interface</td>
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<td>Inter-Integrated Circuit</td>
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<td>Multichannel Audio Serial Port</td>
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<tr>
<td>Multichannel Buffered Serial Port</td>
<td>McBSP</td>
<td>SPRU580</td>
<td>√</td>
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<tr>
<td>Phase-Locked Loop Controller</td>
<td>PLL</td>
<td>SPRU233</td>
<td>√</td>
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<tr>
<td>Program and Data Memory Controller/Direct Memory Access Controller</td>
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<td>SPRU577</td>
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<tr>
<td>Timer, 32-bit</td>
<td>Timer</td>
<td>SPRU582</td>
<td>√</td>
</tr>
<tr>
<td>Two-Level Internal Memory</td>
<td>Cache</td>
<td>SPRU609</td>
<td>√</td>
</tr>
</tbody>
</table>
2 Boot Modes and Configuration

The boot modes and device configuration used by the TMS320C620x/C670x DSPs of the C6000 DSP family are described in SPRU642. It also describes the available boot processes and explains how the device is reset.

3 Enhanced Direct Memory Access (EDMA) Controller

The enhanced direct memory access (EDMA) controller handles all data transfers between the level-two (L2) cache/memory controller and the device peripherals on the TMS320C621x/C671x DSP and TMS320C64x™ DSP. These data transfers include cache servicing, non-cacheable memory accesses, user-programmed data transfers, and host accesses.

The EDMA controller in the C621x/C671x DSP and C64x™ DSP has a different architecture from the previous DMA controller in the TMS320C620x/C670x devices. The EDMA includes several enhancements to the DMA, such as 64 channels for the C64x DSP or 16 channels for the C621x/C671x DSP, with programmable priority, and the ability to link and chain data transfers. The EDMA allows movement of data to/from any addressable memory spaces, including internal memory (L2 SRAM), peripherals, and external memory.

The EDMA has the capability of performing fast and efficient transfers by accepting a quick DMA (QDMA) request from the CPU. A QDMA transfer is best suited for applications that require quick data transfers, such as data requests in a tight loop algorithm.

4 Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module

The Ethernet Media Access Controller (EMAC) controls the flow of packet data from the DSP to the Physical layer (PHY) device. The Management Data Input/Output (MDIO) module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the DSP through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module is also used to control device reset, interrupts, and system priority.
5 Expansion Bus (XBUS)

The expansion bus (XBUS) is a 32-bit wide bus used by the CPU to access off-chip peripherals, FIFOs, and peripheral component interconnect (PCI) interface devices in some of the C62x™ DSPs.

The XBUS has two major subblocks, the I/O port and host port interface. The I/O port has two modes of operation that can coexist in a single system: asynchronous I/O mode and synchronous FIFO mode. The asynchronous I/O mode provides output strobes that are highly programmable, like the asynchronous signals of the external memory interface (EMIF). The FIFO mode provides a glueless interface to a single synchronous read FIFO or up to four synchronous write FIFOs. Connectivity of the XBUS I/O port and DSP memory is provided through the direct-memory access (DMA) controller.

The host port interface can operate in one of two modes: synchronous and asynchronous. The synchronous mode offers master and slave functionality, and has multiplexed address and data signals. The asynchronous mode is slave only and is similar to the host-port interface (HPI) on the C6201/C6211/C6701/C6711 DSP, but is extended to a 32-bit data path. The asynchronous mode is used to interface to microprocessors that utilize an asynchronous bus. Connectivity of the XBUS host port interface and the DSP memory space is provided by the DMA auxiliary port.
6 External Memory Interface (EMIF)

The external memory interfaces (EMIFs) of all C6000 devices support a glueless interface to a variety of external devices, including:

- Pipelined synchronous-burst SRAM (SBSRAM)
- Synchronous DRAM (SDRAM)
- Asynchronous devices, including SRAM, ROM, and FIFOs
- An external shared-memory device

The C620x/C670x EMIF services requests of the external bus from four requestors:

- On-chip program memory controller that services CPU program fetches
- On-chip data memory controller that services CPU data fetches
- On-chip direct-memory access (DMA) controller
- External shared-memory device controller (using EMIF arbitration signals)

If multiple requests arrive simultaneously, the EMIF prioritizes them and performs the necessary number of operations. The C620x/C670x EMIF has a 32-bit data bus interface.

The C621x/C671x EMIF and C64x EMIF service requests of the external bus from two requestors:

- On-chip enhanced direct-memory access (EDMA) controller
- External shared-memory device controller

The C64x EMIF offers additional flexibility by replacing the SBSRAM mode with a programmable synchronous mode, which supports glueless interfaces to the following:

- ZBT (zero bus turnaround) SRAM
- Synchronous FIFOs
- Pipeline and flow-through SBSRAM

The C64x DSP may have two EMIFs, EMIFA and EMIFB.

- EMIFA: Data bus width is device specific.
- EMIFB: 16-bit data bus interface (C6414/C6415/C6416 DSP only).
7 General-Purpose Input/Output (GPIO)

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce CPU interrupts and EDMA events in different interrupt/event generation modes.

8 Host Port Interface (HPI)

The host port interface (HPI) is a parallel port through which a host processor can directly access the CPU memory space. The host device functions as a master to the interface, which increases ease of access. The host and CPU can exchange information via internal or external memory. The host also has direct access to memory-mapped peripherals. Connectivity to the CPU memory space is provided through the direct memory access (DMA) or enhanced DMA (EDMA) controller. Both the host and the CPU can access the HPI control register (HPIC). The host can access the HPI address register (HPIA), the HPI data register (HPID), and the HPIC by using the external data and interface control signals. For the C64x DSP, the CPU can also access the HPIA.

Through the HPI, an external host is capable of accessing the entire DSP memory map except the following:

- L2 control registers (C6x1x DSP only)
- Interrupt selector registers
- Emulation logic
9 Inter-INtegrated Circuit (I2C) Module

The inter-integrated circuit (I2C) module provides an interface between a C6000 DSP and I2C-compatible devices connected by way of the I2C serial bus. External components attached to the I2C bus serially transmit/receive up to 8-bit data to/from the C6000 DSP through the 2-wire I2C interface. The I2C module has the following features:

The I2C module has the following features:

- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
  - Support for byte format transfer
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (Philips Fast-mode rate)

- One read EDMA event and one write EDMA event, which can be used by the EDMA controller

- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions: transmit-data ready, receive-data ready, register-access ready, no-acknowledgement received, arbitration lost.

- Module enable/disable capability

- Free data format mode

The I2C module of the C6410/C6413/C6418 DSP offers the following additional features:

- The SDA and SCL pins can be used for general-purpose input/output (GPIO) through the use of six additional registers.

- Two additional status bits in the I2C status register (I2CSTR).

- Two additional interrupts enabled in the I2C interrupt enable register (I2CIER).

- Two different ways to generate a transmit data ready interrupt when operating in slave-transmitter mode and enabled by the I2C extended mode register (I2CEMDR).
10 Interrupt Selector

The C6000 DSP peripheral set has up to 32 interrupt sources; however, the CPU has 12 interrupts available for use. The interrupt selector allows you to choose and prioritize which 12 of the 32 your system needs to use. The interrupt selector also allows you to effectively change the polarity of external interrupt inputs.

The interrupt selector, interrupt selector registers, and the available interrupts in the DSPs of the C6000 DSP family are described in this document.

11 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for both Inter-Integrated Sound (IIS) protocols and inter-component digital audio interface transmission (DIT).

The McASP is intended to be flexible so that it may connect gluelessly to audio analog-to-digital converters (ADC), digital-to-analog converters (DAC), codec, digital audio interface receiver (DIR), and S/PDIF transmit physical layer components.

Features of the McASP include:

- Two independent clocks (transmit and receive)
- 16 serial data pins, individually assignable
- Each clock includes:
  - Programmable clock generator
  - Programmable frame sync generator
  - TDM streams from 2 to 32, and 384 time slots
  - Support for slot sizes of 8, 12, 16, 20, 24, 28, and 32 bits
  - Data formatter for bit manipulation
- Wide variety of IIS and similar bit stream format
- Integrated digital audio interface transmitter (DIT) supports:
  - S/PDIF, IEC60958-1, AES-3 formats
  - Up to 16 transmit pins
  - Enhanced channel status/user data RAM
- Extensive error checking and recovery
12 Multichannel Buffered Serial Port (McBSP)

The multichannel buffered serial port (McBSP) is based on the standard serial port interface found on the TMS320C2000™ and TMS320C5000™ platforms. In addition, the port can buffer serial samples in memory automatically with the aid of the DMA/EDMA controller. It also has multichannel capability compatible with the T1, E1, SCSA, and MVIP networking standards. The McBSP provides these functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- External shift clock or an internal, programmable frequency shift clock for data transfer
- Autobuffering capability through the 5-channel DMA controller

In addition, the McBSP has the following capabilities:

- Direct interface to:
  - T1/E1 framers
  - MVIP switching compatible and ST-BUS compliant devices including:
    - MVIP framers
    - H.100 framers
    - SCSA framers
  - IOM-2 compliant devices
  - AC97 compliant devices (The necessary multi phase frame synchronization capability is provided.)
  - IIS compliant devices
  - SPI™ devices
- Multichannel transmit and receive of up to 128 channels
- A wide selection of data sizes, including 8, 12, 16, 20, 24, and 32 bits
- μ-Law and A-Law companding
- 8-bit data transfers with the option of LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation

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13 Peripheral Component Interconnect (PCI)

The peripheral component interconnect (PCI) port supports connection of the C6000 DSP to a PCI host via the integrated PCI master/slave bus interface. For C62x devices, the PCI port interfaces to the DSP via the auxiliary channel of the DMA controller. For C64x devices, the PCI port interfaces to the DSP via the enhanced DMA (EDMA) controller. This architecture allows for both PCI master and slave transactions, while keeping the DMA/EDMA channel resources available for other applications.

The C62x PCI port provides the auxiliary DMA with a source/destination address in the DSP memory. Address decode is performed by the DMA to select the appropriate interface (data memory, program memory, register I/O, or external memory). The auxiliary channel of the DMA controller should be programmed for the highest priority in order to achieve the maximum throughput on the PCI interface.

The C64x PCI port uses the EDMA internal address generation hardware to perform address decode instead.

14 Phase-Locked Loop (PLL) Controller

The phase-locked loop (PLL) controller in some of the C6000 DSPs features a software-configurable PLL multiplier controller, dividers, and reset controller. The PLL controller accepts an input clock, as determined by the logic state on the CLKMODE0 pin, from the CLKin pin or from the on-chip oscillator output signal OSCIN. The PLL controller offers flexibility and convenience by way of a software-configurable multiplier and dividers to modify the input signal internally. The resulting clock outputs are passed to the DSP core, peripherals, and other modules inside the C6000 DSP.

15 Program and Data Memory Controller/Direct Memory Access (DMA) Controller

The C6201/C6204/C6205/C6701 DSP internal program memory is user-configurable as cache or memory-mapped program space. It contains 64K bytes of RAM or, equivalently, 2K 256-bit fetch packets or 16K 32-bit instructions. The CPU, through the program memory controller, has a single-cycle throughput, 256-bit-wide connection to internal program memory.

In the C6202(B)/C6203(B) DSP, the memory/cache program space is expanded. In addition, the C6202(B)/C6203(B) DSP provides another block of memory that operates as a memory-mapped block. These two blocks can be accessed independently. This allows the CPU to perform program fetch from one block of program memory, without interfering with a DMA transfer from the other block.
The program memory controller performs the following tasks:

- Performs CPU and DMA requests to internal program memory and the necessary arbitration.
- Performs CPU requests to external memory through the external memory interface (EMIF).
- Manages the internal program memory when it is configured as cache.

The data memory controller connects:

- The CPU and direct memory access (DMA) controller to internal data memory and performs the necessary arbitration.
- The CPU to the external memory interface (EMIF).
- The CPU to the on-chip peripherals through the peripheral bus controller.

The peripheral bus controller performs arbitration between the CPU and DMA for the on-chip peripherals.

The DMA controller transfers data between regions in the memory map without intervention by the CPU. The DMA controller allows movement of data to and from internal memory, internal peripherals, or external devices to occur in the background of CPU operation. The DMA controller has four independent programmable channels, allowing four different contexts for DMA operation. In addition, a fifth (auxiliary) channel allows the DMA controller to service requests from the host port interface (HPI). Requests are sent to one of these possible resources:

- Expansion bus (C6202/C6203/C6204 DSP only)
- Host port interface (C6201/C6701 DSP only)
- PCI (C6205 DSP only)
- External memory interface
- Internal program memory, block 0
- Internal program memory, block 1 (C6202/C6203 DSP only)
- Internal peripheral bus
- Internal data memory
16 Timer

The C6000 DSP device has 32-bit general-purpose timers that can be used to:

- Time events
- Count events
- Generate pulses
- Interrupt the CPU
- Send synchronization events to the DMA

The timers have two signaling modes and can be clocked by an internal or an external source. The timers have an input pin and an output pin. The input and output pins (TINP and TOUT) can function as timer clock input and clock output. They can also be respectively configured for general-purpose input and output.

With an internal clock, for example, the timer can signal an external A/D converter to start a conversion, or it can trigger the DMA controller to begin a data transfer. With an external clock, the timer can count external events and interrupt the CPU after a specified number of events.

17 Turbo Decoder Coprocessor (TCP)

Channel decoding of high bit-rate data channels found in third generation (3G) cellular standards requires decoding of turbo-encoded data. The turbo decoder coprocessor (TCP) is designed to perform this operation for IS2000 and 3GPP wireless standards. The TCP provides:

- High performance:
  - Very low processing delay thanks to a highly paralleled architecture allowing 8 iterations of a 2Mbps 3GPP channel to be decoded in less than 2 ms and a 1Mbps IS-2000 channel in less than 3.5 ms.
  - Processing delay can be further reduced by enabling a stopping criteria algorithm.
  - TCP and DSP can run full speed in parallel.

- System cost optimization:
  - Reduces board space and power consumption by performing turbo-decoding on-chip.
  - Communication between the DSP and the TCP is performed through a high performance DMA engine, the EDMA.
  - TCP uses its own optimized working memories.
High flexibility to cope with standard evolutions:
- Accepts all IS2000, 3GPP rates and polynomials.
- Accepts any frame length from 40 (3GPP minimum frame size) up to 20730 (IS2000 maximum frame size).
- Can use any kind of interleaver.
- Frees-up DSP resources.

The TCP has two fundamental modes: standalone (SA) and shared processing (SP). In SA mode, the TCP iterates a given number of times and outputs hard-decisions. In SP mode, the TCP executes a single MAP decode and outputs extrinsic information (soft information). SA mode is typically used for frame sizes smaller or equal to 5114; whereas, SP mode must be used for frames strictly larger than 5114.

18 Two-Level Internal Memory

The C621x/C671x DSP and C64x DSP have a two-level memory architecture for program and data. The first-level program cache is designated L1P, and the first-level data cache is designated L1D. Both the program and data memory share the second-level memory, designated L2. L2 is configurable, allowing for various amounts of cache and SRAM.

The level 1 data cache (L1D) services data accesses from the CPU. The level 1 program cache (L1P) services program fetches from the CPU. The level 2 unified memory (L2) can operate as SRAM, cache, or both. It services cache misses from both L1P and L1D, as well as DMA accesses using the EDMA controller.

19 Universal Test and Operations PHY Interface for ATM (UTOPIA)

The universal test and operations PHY interface for asynchronous transfer mode [ATM] (UTOPIA) peripheral in the C6415/C6416 DSP is an ATM controller (ATMC) slave device that interfaces to a master ATM controller. The UTOPIA port conforms to the ATM Forum standard specification af-phy-0039.000. Specifically, this interface supports the UTOPIA Level 2 interface that allows 8-bit slave operation up to 50 MHz for both transmit and receive operations.

The UTOPIA slave interface relies on the master ATM controller to provide the necessary control signals such as the clock, enable and address values. Only cell-level handshaking is supported.

Both the CPU and enhanced DMA (EDMA) controller can service the UTOPIA. The UTOPIA slave consists of the transmit interface and the receive interface. The UTOPIA sends notification of interrupts to the CPU via the UINT signal and synchronization events to the EDMA controller via the UXEVGT and UREVGT signals.
20  Video Port/VCXO Interpolated Control (VIC) Port

The video port peripheral can operate as a video capture port, video display port, or transport stream interface (TSI) capture port. The video port consists of two channels: A and B. A 5120-byte capture/display buffer is splittable between the two channels. The entire port (both channels) is always configured for either video capture or video display only. Separate data pipelines control the parsing and formatting of video capture or video display data for each of the BT.656, Y/C, raw video, and TSI modes.

For video capture operation, the video port may operate as two 8/10-bit channels of BT.656 or raw video capture; or as a single channel of 8/10-bit BT.656, 8/10-bit raw video, 16/20-bit Y/C video, 16/20-bit raw video, or 8-bit TSI.

For video display operation, the video port may operate as a single channel of 8/10-bit BT.656, 8/10-bit raw video, 16/20 bit Y/C video, or 16/20-bit raw video. It may also operate in a two channel 8/10-bit raw mode in which the two channels are locked to the same timing. Channel B is not used during single channel operation.

The VCXO interpolated control (VIC) port provides single-bit interpolated VCXO control with resolution from 9 bits to up to 16 bits. The frequency of interpolation is dependent on the resolution needed. When the video port is used in TSI mode, the VIC port is used to control the system clock, VCXO, for MPEG transport stream. The VIC port supports following features:

- Single-bit interpolated VCXO control
- Programmable precision from 9 to 16 bits
21 Viterbi Decoder Coprocessor (VCP)

Channel decoding of voice and low bit-rate data channels found in third generation (3G) cellular standards requires decoding of convolutional encoded data. The Viterbi-decoder coprocessor (VCP) is designed to perform this operation for IS2000 and 3GPP wireless standards. The VCP provides:

- High flexibility:
  - variable constraint length K = 5, 6, 7, 8 or 9
  - user supplied code coefficients
  - code rates (1/2, 1/3, 1/4)
  - configurable trace back settings (convergence distance, frame structure)
  - branch metrics calculation and depuncturing done in software by the DSP
  - frees-up DSP resources for other processing

- System cost optimization:
  - Reduces board space and power consumption by performing decoding on-chip
  - Communication between the DSP and the VCP is performed through a high performance DMA engine
  - VCP uses its own optimized working memories

The DSP controls the operation of the VCP using memory-mapped registers. The DSP typically sends and receives data using synchronized EDMA transfers through the 64-bit EDMA bus. The VCP sends two synchronization events to the EDMA: a read event (VCPREVT) and a write event (VCPXEVТ).